FIG. 1

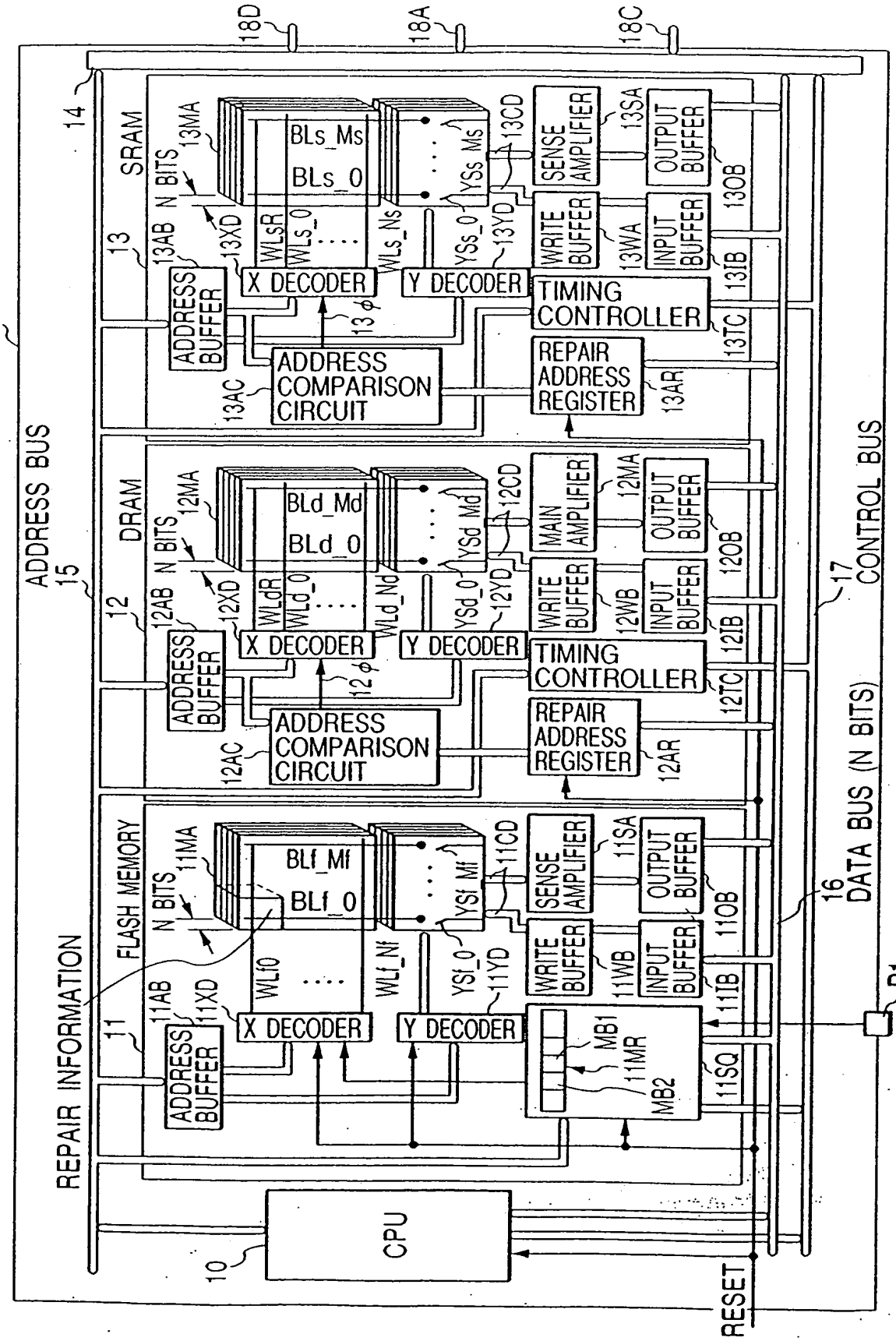

ADDRESS BUS
DATA BUS (N BITS)
CONTROL BUS
REPAIR INFORMATION
RESET
CPU
SRAM
DRAM
FLASH MEMORY
X DECODER
Y DECODER
ADDRESS BUFFER
ADDRESS COMPARISON CIRCUIT
REPAIR ADDRESS REGISTER
TIMING CONTROLLER
SENSE AMPLIFIER
MAIN AMPLIFIER
WRITE BUFFER
INPUT BUFFER
OUTPUT BUFFER
N BITS
P1

FIG. 2

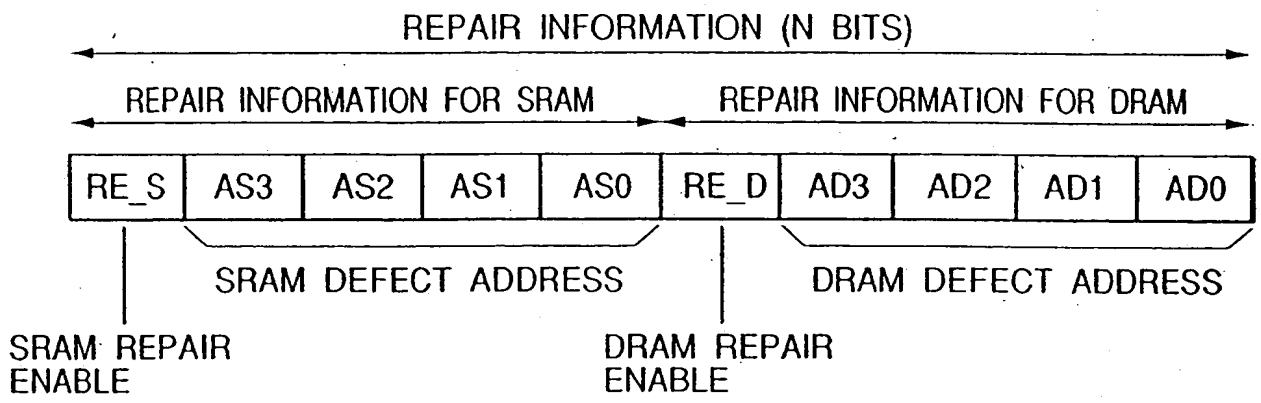

REPAIR INFORMATION (N BITS)
REPAIR INFORMATION FOR SRAM
REPAIR INFORMATION FOR DRAM
RE_S
AS3
AS2
AS1
AS0
RE_D
AD3
AD2
AD1
AD0
SRAM DEFECT ADDRESS
DRAM DEFECT ADDRESS
SRAM REPAIR ENABLE
DRAM REPAIR ENABLE

FIG. 3

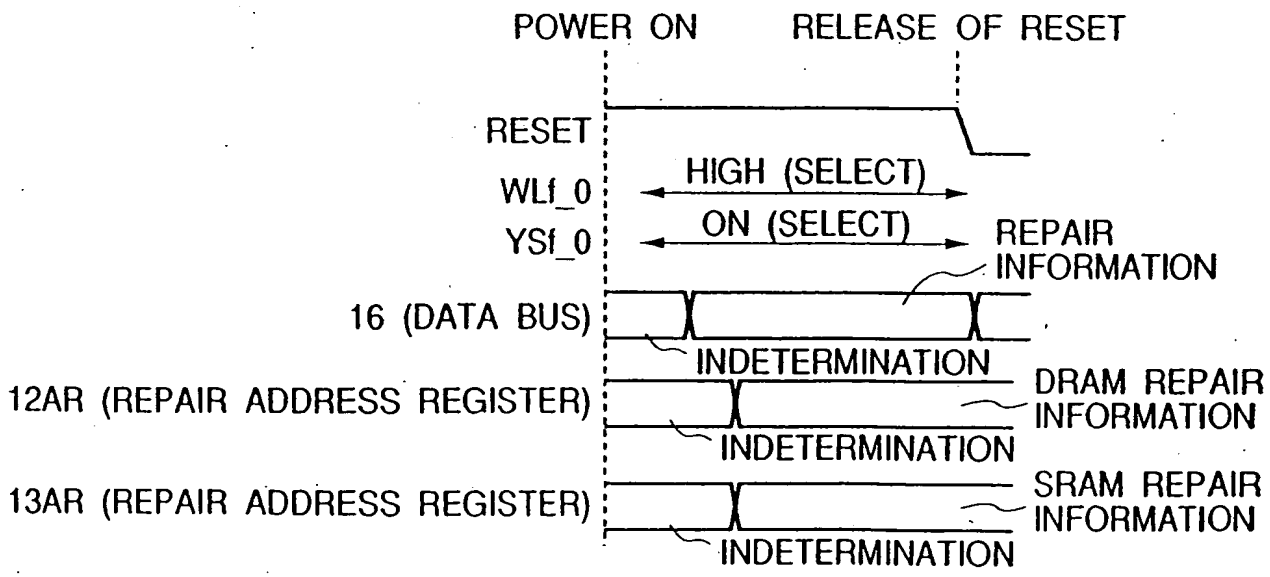

POWER ON
RELEASE OF RESET
RESET
WLi_0
HIGH (SELECT)
YSi_0
ON (SELECT)
REPAIR INFORMATION
16 (DATA BUS)
INDETERMINATION
12AR (REPAIR ADDRESS REGISTER)
DRAM REPAIR INFORMATION
INDETERMINATION
13AR (REPAIR ADDRESS REGISTER)
SRAM REPAIR INFORMATION
INDETERMINATION

FIG. 4(A)

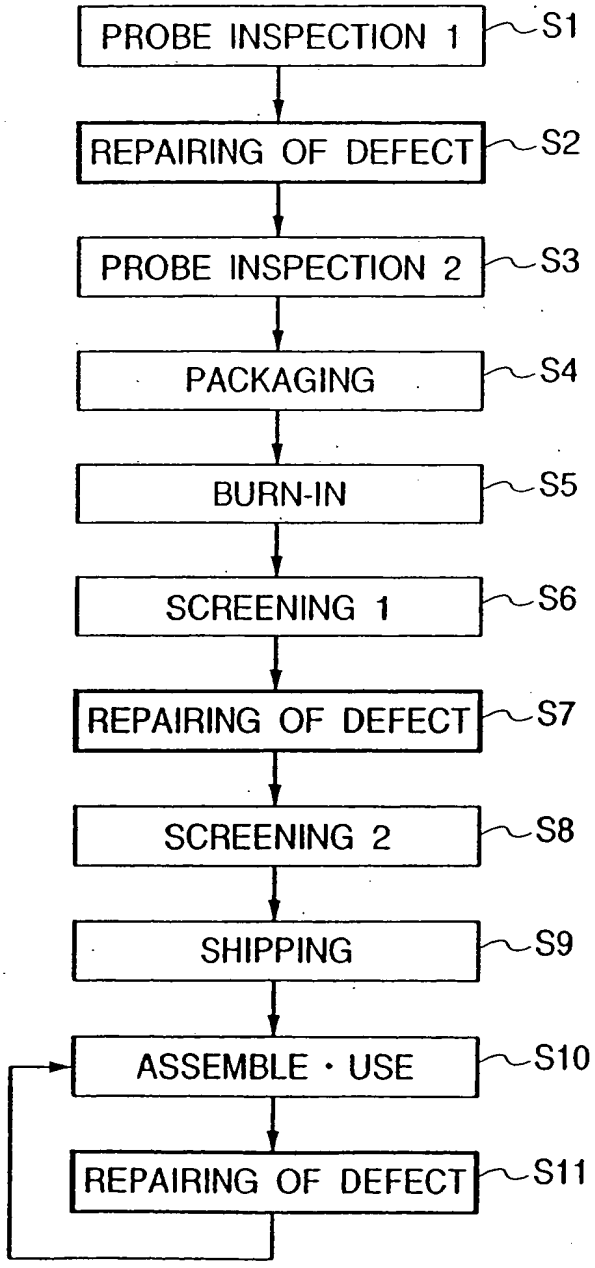

PROBE INSPECTION 1
S1
REPAIRING OF DEFECT
S2
PROBE INSPECTION 2
S3
PACKAGING
S4
BURN-IN
S5
SCREENING 1
S6
REPAIRING OF DEFECT
S7
SCREENING 2
S8
SHIPPING
S9
ASSEMBLE · USE
S10
REPAIRING OF DEFECT
S11

FIG. 4(B)

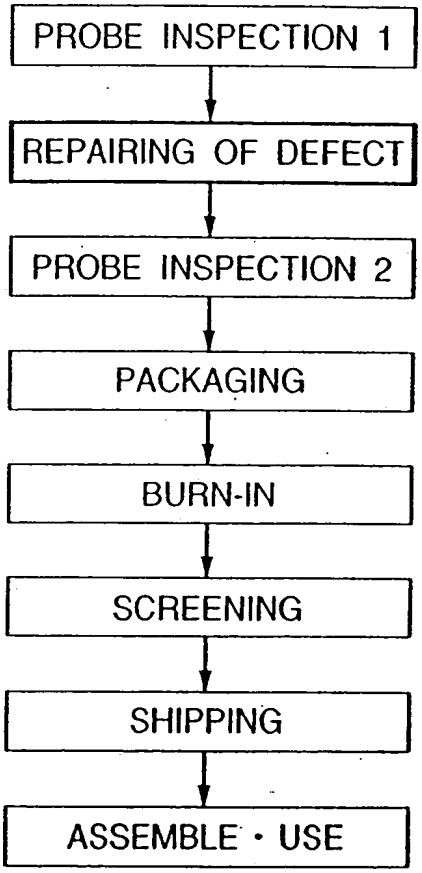

PROBE INSPECTION 1
REPAIRING OF DEFECT
PROBE INSPECTION 2
PACKAGING
BURN-IN
SCREENING
SHIPPING
ASSEMBLE · USE

FIG. 5

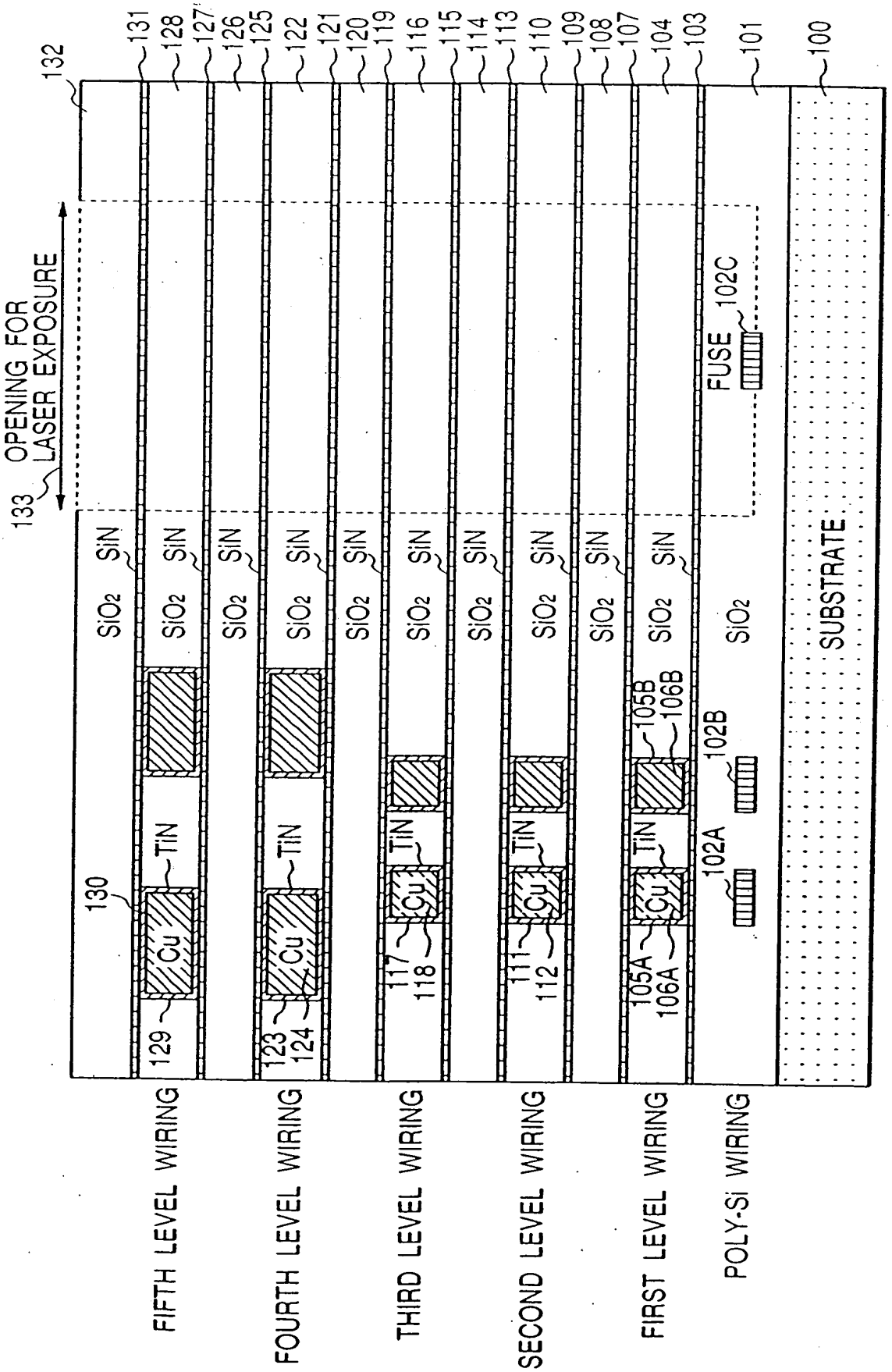

132
131
128
127
126
125
122
121
120
119
116
115
114
113
110
109
108
107
104
103
101
100
OPENING FOR LASER EXPOSURE
133
SiO2
SiN
TiN
Cu
130
129
123
124
117
118
111
112
105A
106A
105B
106B
102A
102B
FUSE
102C
SUBSTRATE
FIFTH LEVEL WIRING
FOURTH LEVEL WIRING
THIRD LEVEL WIRING
SECOND LEVEL WIRING
FIRST LEVEL WIRING
POLY-Si WIRING

FIG. 6

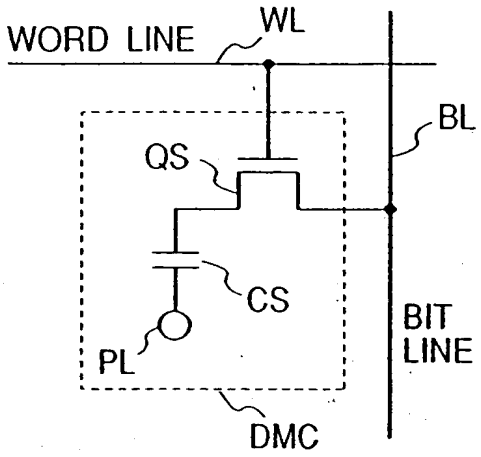

WORD LINE
WL
BL
QS
CS
PL
BIT
LINE
DMC

FIG. 8

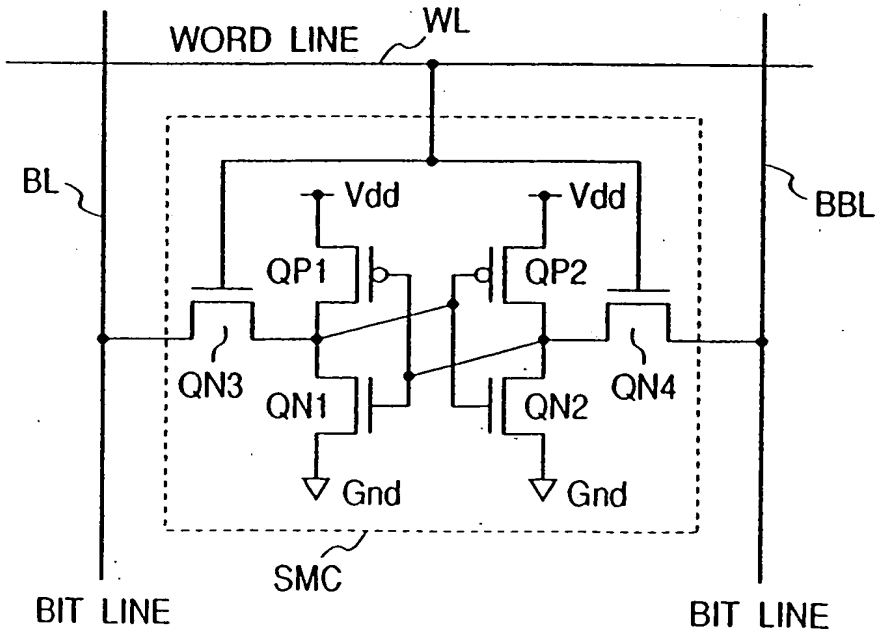

WORD LINE
WL
BL
BBL
Vdd
Vdd
QP1
QP2
QN3
QN1
QN2
QN4
Gnd
Gnd
SMC
BIT LINE
BIT LINE

FIG. 7

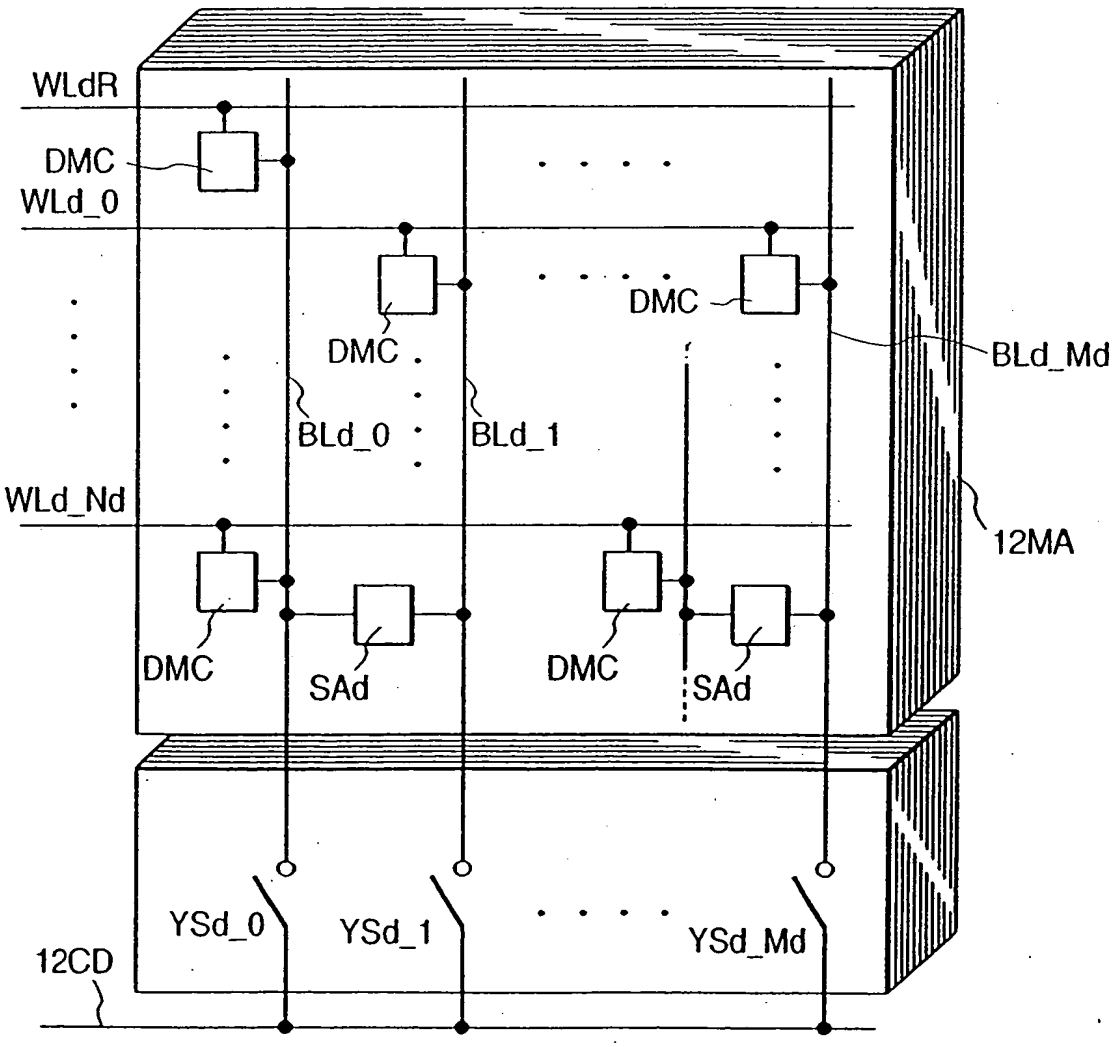

WLdR
DMC
WLd_0
DMC
DMC
BLd_Md
BLd_0
BLd_1
WLd_Nd
12MA
DMC
SAd
DMC
SAd
YSd_0
YSd_1
YSd_Md
12CD

FIG. 9

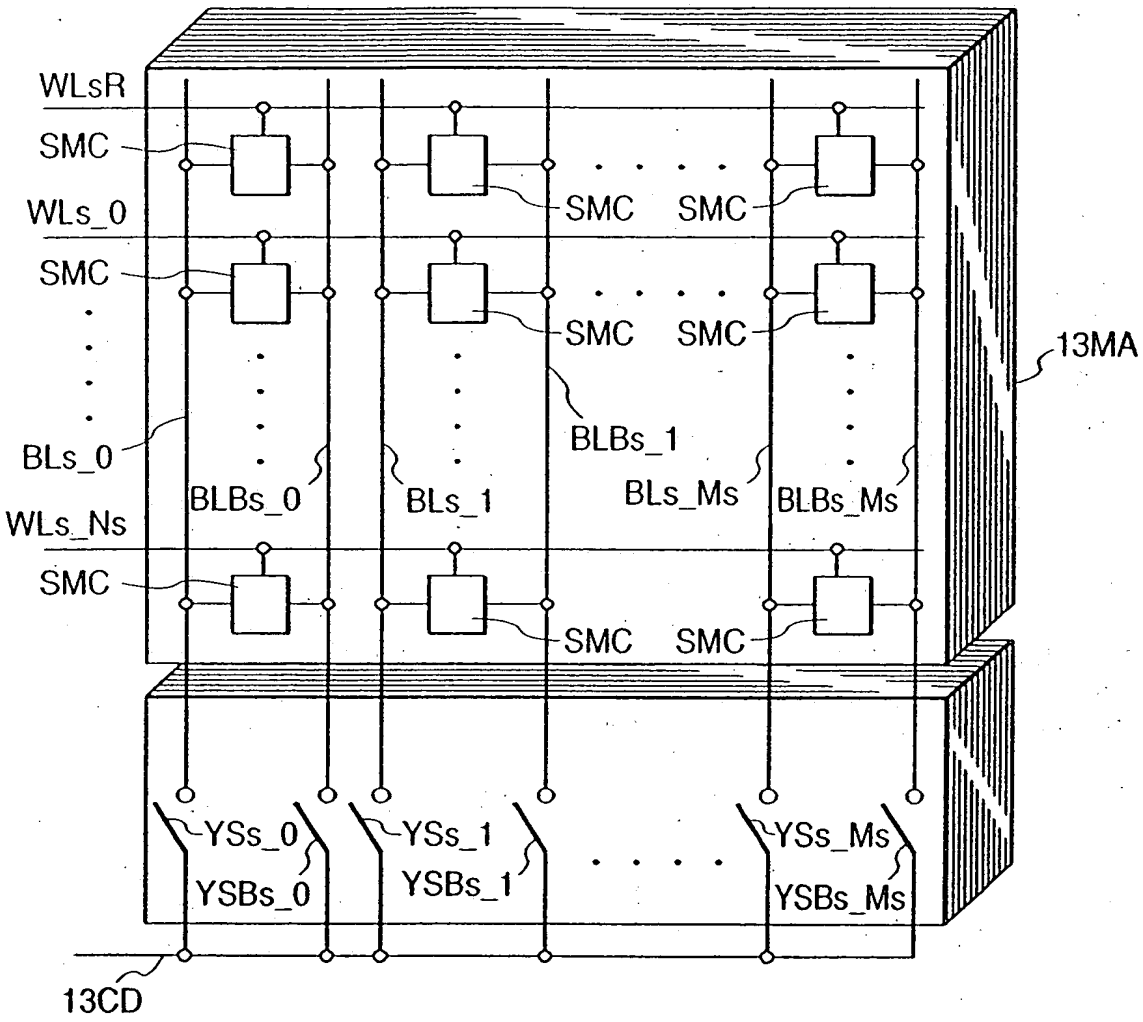

WLsR
SMC
WLs_0
SMC
BLs_0
WLs_Ns
SMC
BLBs_0
BLs_1
BLBs_1
BLs_Ms
BLBs_Ms
13MA
YSs_0
YSBs_0
YSs_1
YSBs_1
YSs_Ms
YSBs_Ms
13CD

FIG. 10

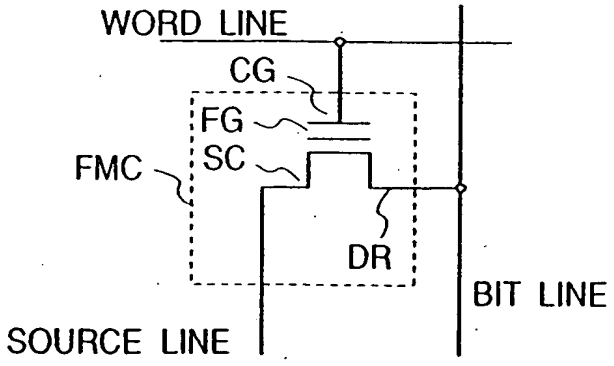

WORD LINE
CG
FG
SC
FMC
DR
BIT LINE
SOURCE LINE

FIG. 11

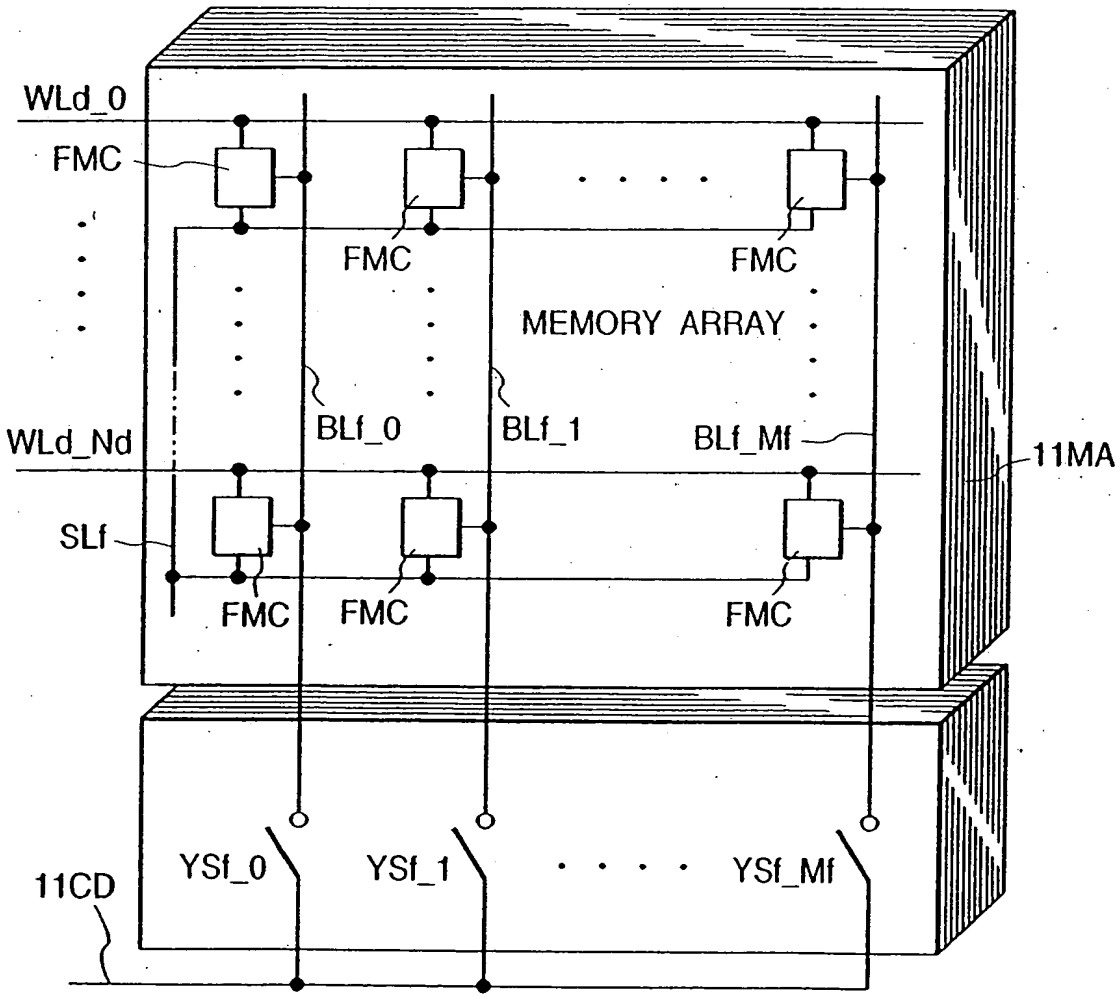

WLd_0
FMC
FMC
FMC
MEMORY ARRAY
WLd_Nd
BLf_0
BLf_1
BLf_Mf
11MA
SLf
FMC
FMC
FMC
YSf_0
YSf_1
YSf_Mf
11CD

FIG. 12

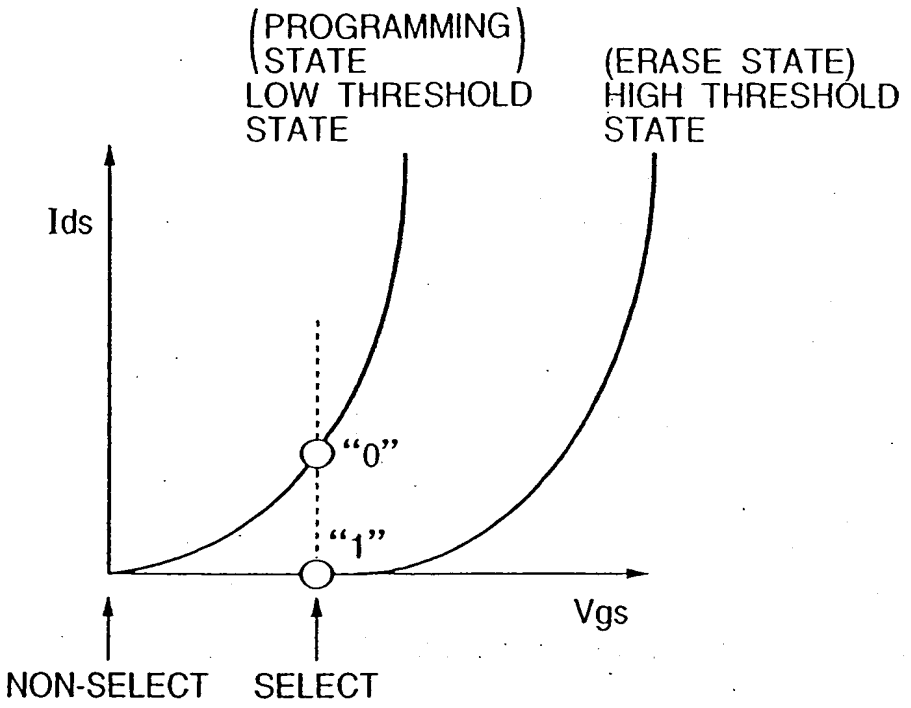


FIG. 13

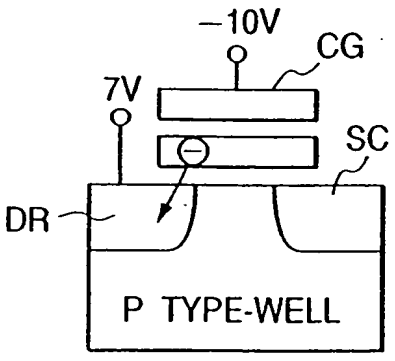
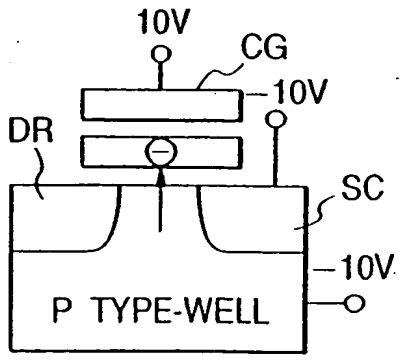
PROGRAMMING OPERATION	ERASE OPERATION
	
LOW THRESHOLD STATE LOGIC VALUE "0"	HIGH THRESHOLD STATE LOGIC VALUE "1"

FIG. 14

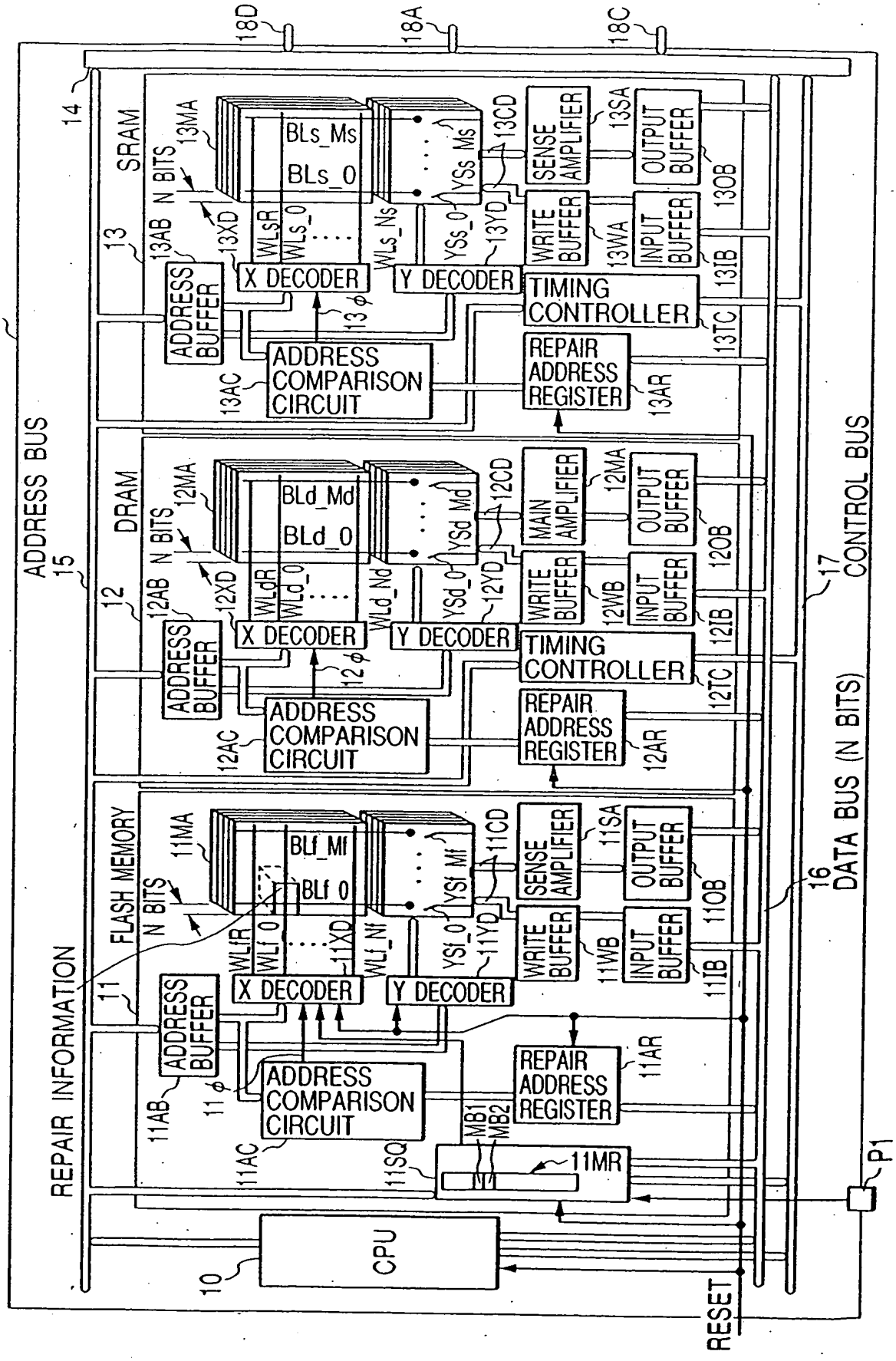

1B
ADDRESS BUS
15
CONTROL BUS
17
DATA BUS (N BITS)
16
REPAIR INFORMATION
18D
18A
18C
14
SRAM
13
13AB
N BITS
13MA
BLs_Ms
BLs_0
13XD
WLsR
WLs_0
WLs_Ns
13CD
YSs_Ms
YSs_0
13YD
SENSE AMPLIFIER
13SA
OUTPUT BUFFER
13OB
WRITE BUFFER
13WA
INPUT BUFFER
13IB
ADDRESS BUFFER
X DECODER
Y DECODER
13φ
TIMING CONTROLLER
13TC
ADDRESS COMPARISON CIRCUIT
13AC
REPAIR ADDRESS REGISTER
13AR
DRAM
12
12AB
N BITS
12MA
BLd_Md
BLd_0
12XD
WLdR
WLd_0
WLd_Nd
12CD
YSd_Md
YSd_0
12YD
MAIN AMPLIFIER
12MA
OUTPUT BUFFER
12OB
WRITE BUFFER
12WB
INPUT BUFFER
12IB
ADDRESS BUFFER
X DECODER
Y DECODER
12φ
TIMING CONTROLLER
12TC
ADDRESS COMPARISON CIRCUIT
12AC
REPAIR ADDRESS REGISTER
12AR
FLASH MEMORY
11
N BITS
11MA
BLf_Mf
BLf_0
11XD
WLfR
WLf_0
WLf_Nf
11CD
YSf_Mf
YSf_0
11YD
SENSE AMPLIFIER
11SA
OUTPUT BUFFER
11OB
WRITE BUFFER
11WB
INPUT BUFFER
11IB
ADDRESS BUFFER
X DECODER
Y DECODER
11φ
11AB
ADDRESS COMPARISON CIRCUIT
11AC
REPAIR ADDRESS REGISTER
11AR
MB1
MB2
11SQ
11MR
CPU
10
P1
RESET

FIG. 15

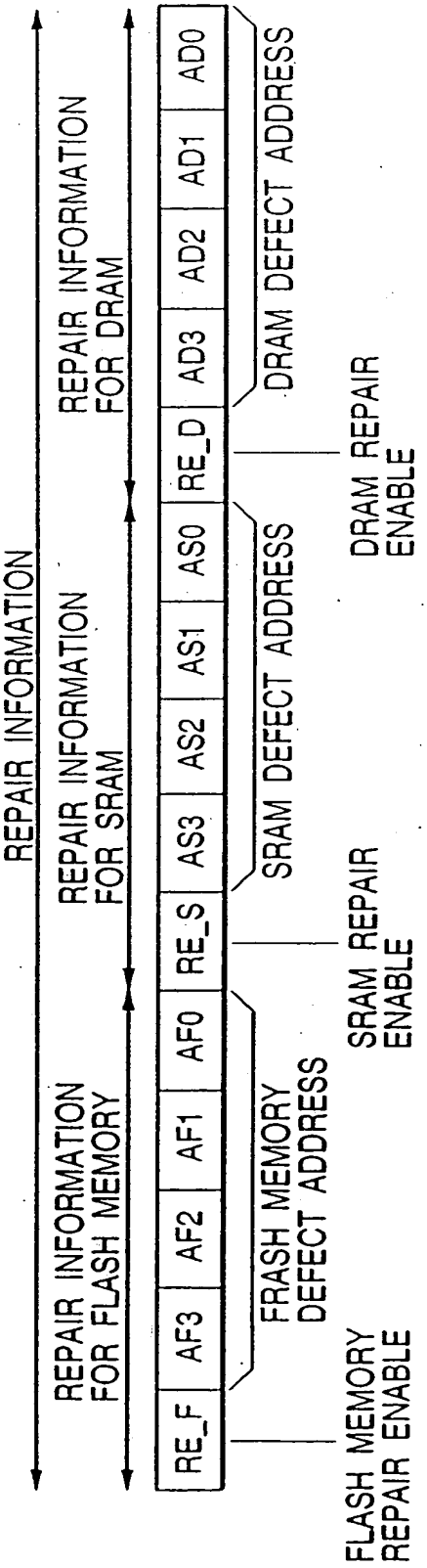

REPAIR INFORMATION
REPAIR INFORMATION FOR DRAM
REPAIR INFORMATION FOR SRAM
REPAIR INFORMATION FOR FLASH MEMORY
RE_F
AF3
AF2
AF1
AF0
RE_S
AS3
AS2
AS1
AS0
RE_D
AD3
AD2
AD1
AD0
FLASH MEMORY REPAIR ENABLE
FRASH MEMORY DEFECT ADDRESS
SRAM REPAIR ENABLE
SRAM DEFECT ADDRESS
DRAM REPAIR ENABLE
DRAM DEFECT ADDRESS

FIG. 16

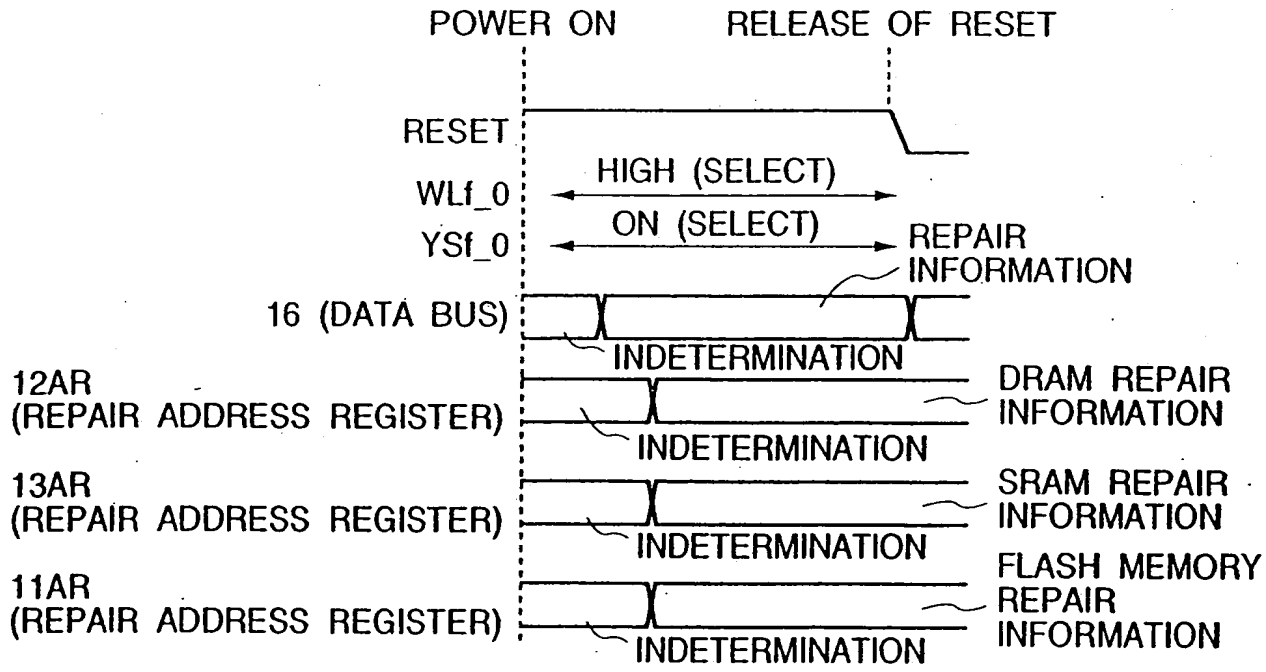

POWER ON
RELEASE OF RESET
RESET
HIGH (SELECT)
WLf_0
ON (SELECT)
YSf_0
REPAIR INFORMATION
16 (DATA BUS)
INDETERMINATION
12AR (REPAIR ADDRESS REGISTER)
DRAM REPAIR INFORMATION
INDETERMINATION
13AR (REPAIR ADDRESS REGISTER)
SRAM REPAIR INFORMATION
INDETERMINATION
11AR (REPAIR ADDRESS REGISTER)
FLASH MEMORY REPAIR INFORMATION
INDETERMINATION

FIG. 17

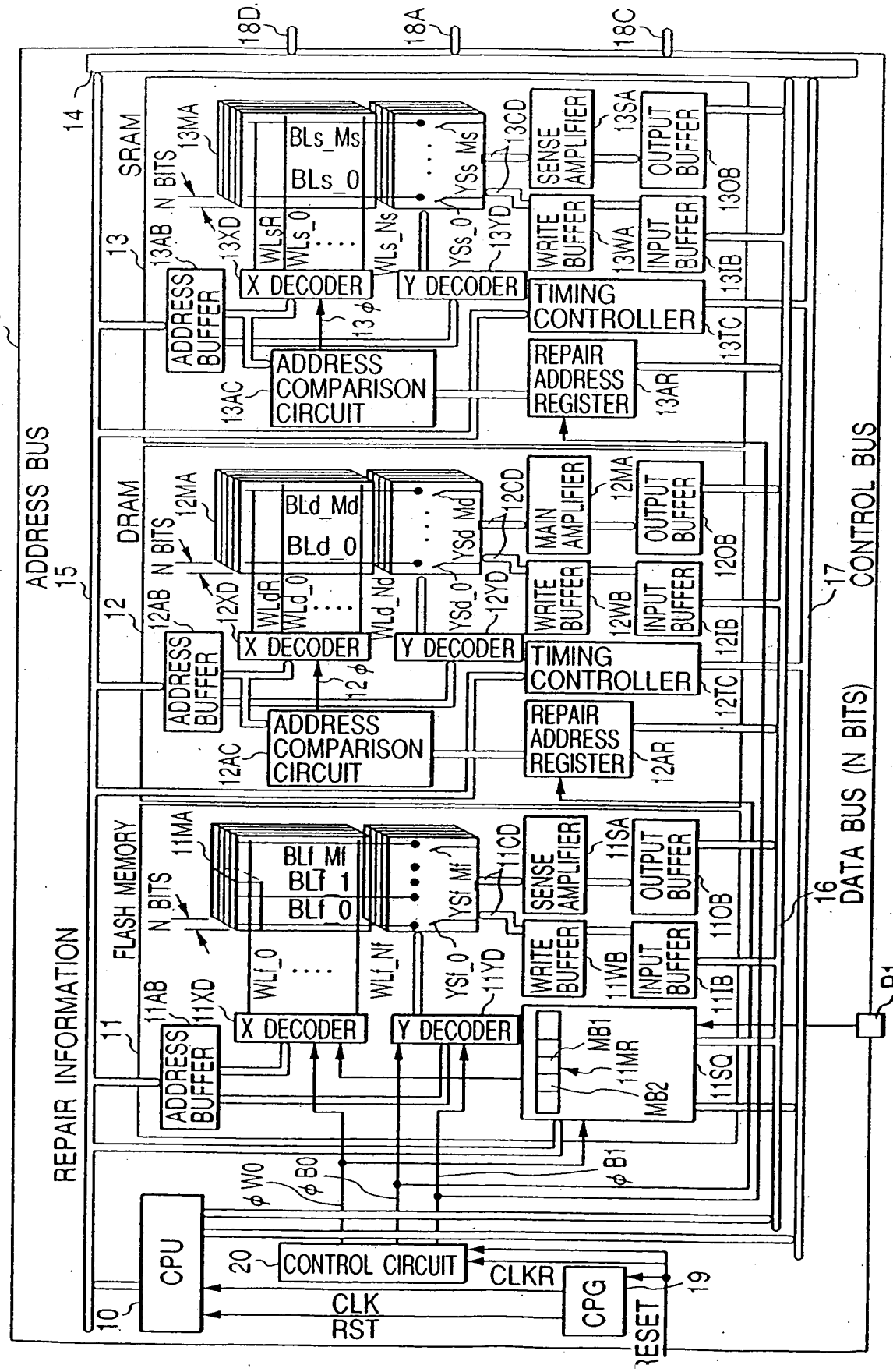

1C
ADDRESS BUS
CONTROL BUS
DATA BUS (N BITS)
REPAIR INFORMATION
SRAM
DRAM
FLASH MEMORY
N BITS
ADDRESS BUFFER
X DECODER
Y DECODER
ADDRESS COMPARISON CIRCUIT
REPAIR ADDRESS REGISTER
TIMING CONTROLLER
SENSE AMPLIFIER
MAIN AMPLIFIER
WRITE BUFFER
INPUT BUFFER
OUTPUT BUFFER
CPU
CONTROL CIRCUIT
CPG
CLK
CLKR
RST
RESET
P1

FIG. 18

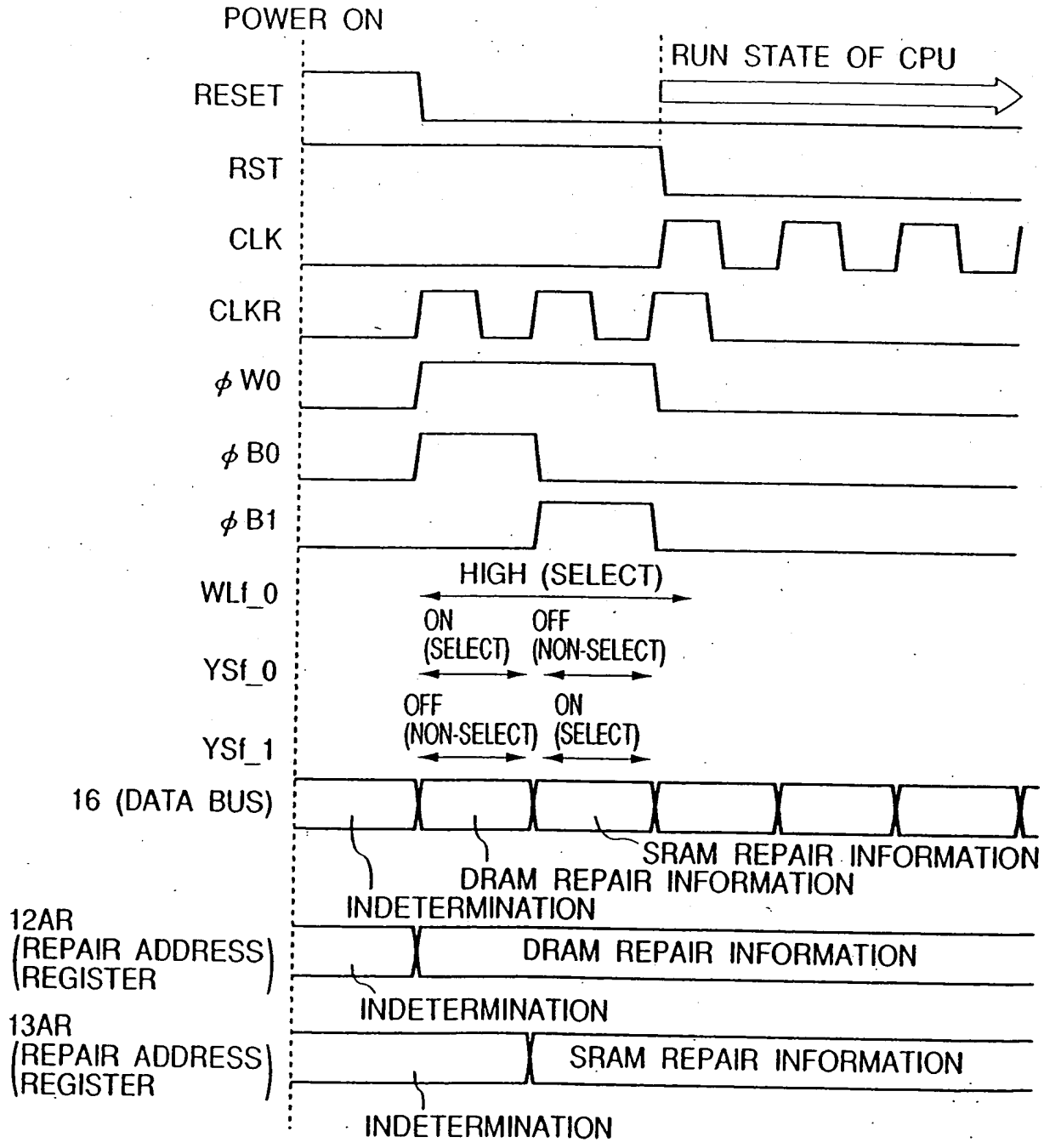

POWER ON
RUN STATE OF CPU
RESET
RST
CLK
CLKR
φ W0
φ B0
φ B1
WLf_0
HIGH (SELECT)
YSf_0
ON (SELECT)
OFF (NON-SELECT)
YSf_1
OFF (NON-SELECT)
ON (SELECT)
16 (DATA BUS)
SRAM REPAIR INFORMATION
DRAM REPAIR INFORMATION
INDETERMINATION
12AR (REPAIR ADDRESS REGISTER)
DRAM REPAIR INFORMATION
INDETERMINATION
13AR (REPAIR ADDRESS REGISTER)
SRAM REPAIR INFORMATION
INDETERMINATION

FIG. 19

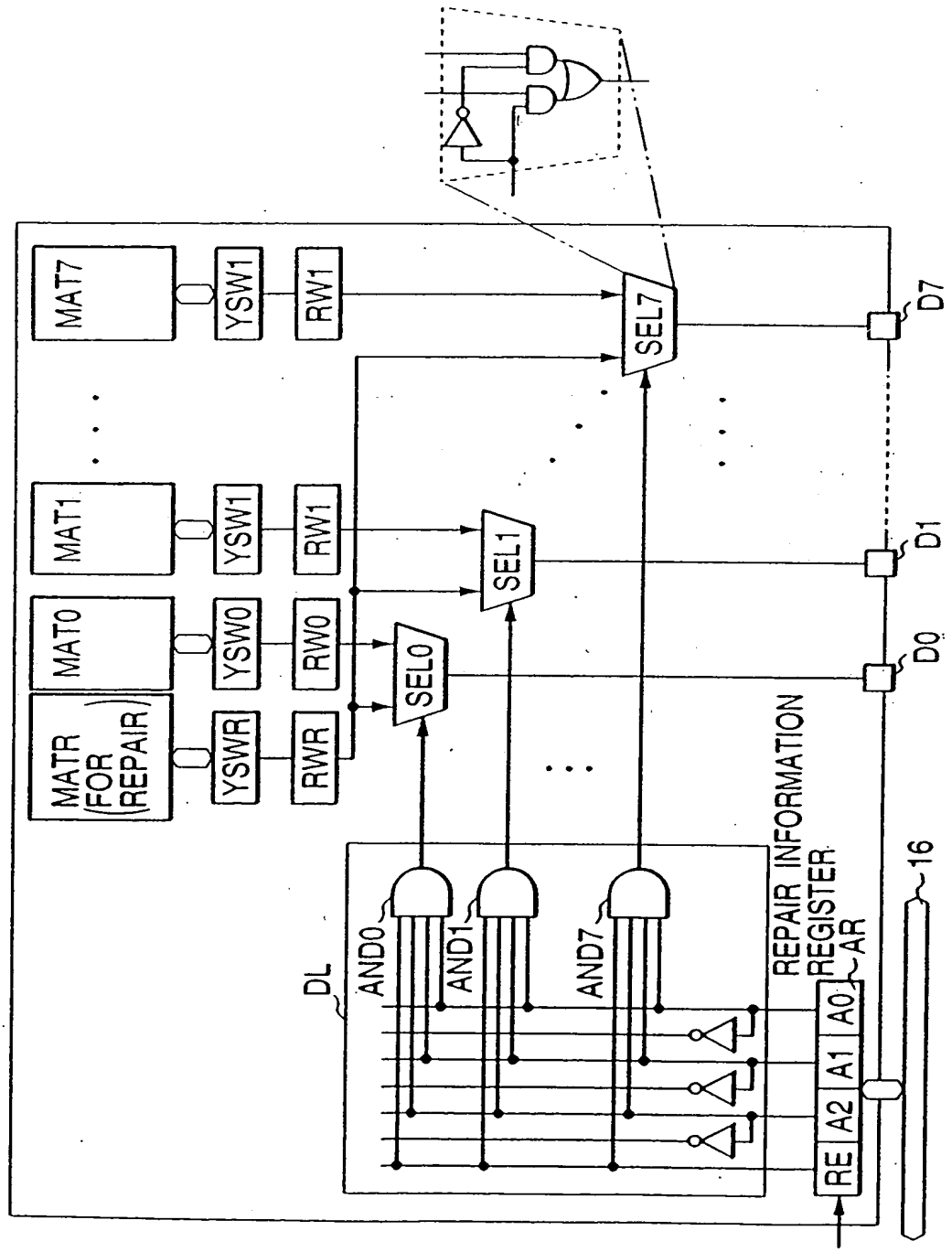

MAT7
MAT1
MAT0
MATR (FOR REPAIR)
YSW1
YSW0
YSWR
RW1
RW0
RWR
SEL7
SEL1
SEL0
D7
D1
D0
DL
AND0
AND1
AND7
REPAIR INFORMATION REGISTER
AR
A0
A1
A2
RE
16

FIG. 20

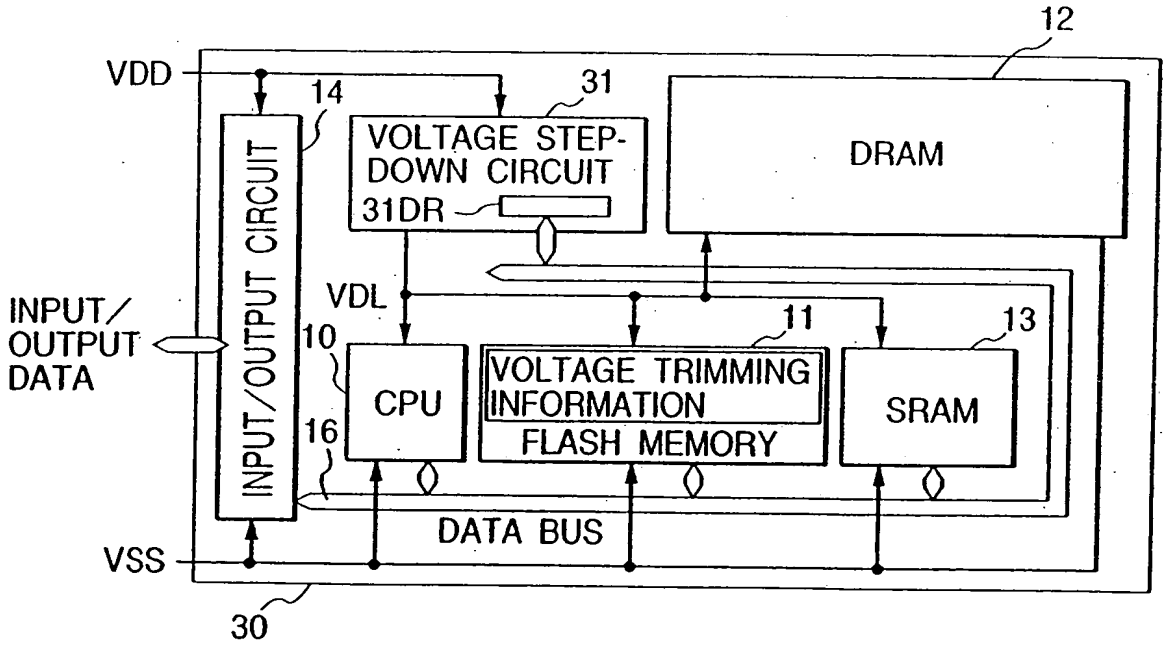

12
VDD
14
31
VOLTAGE STEP-DOWN CIRCUIT
31DR
DRAM
INPUT/OUTPUT CIRCUIT
VDL
INPUT/ OUTPUT DATA
10
11
13
CPU
VOLTAGE TRIMMING INFORMATION
FLASH MEMORY
SRAM
16
DATA BUS
VSS
30

FIG. 21

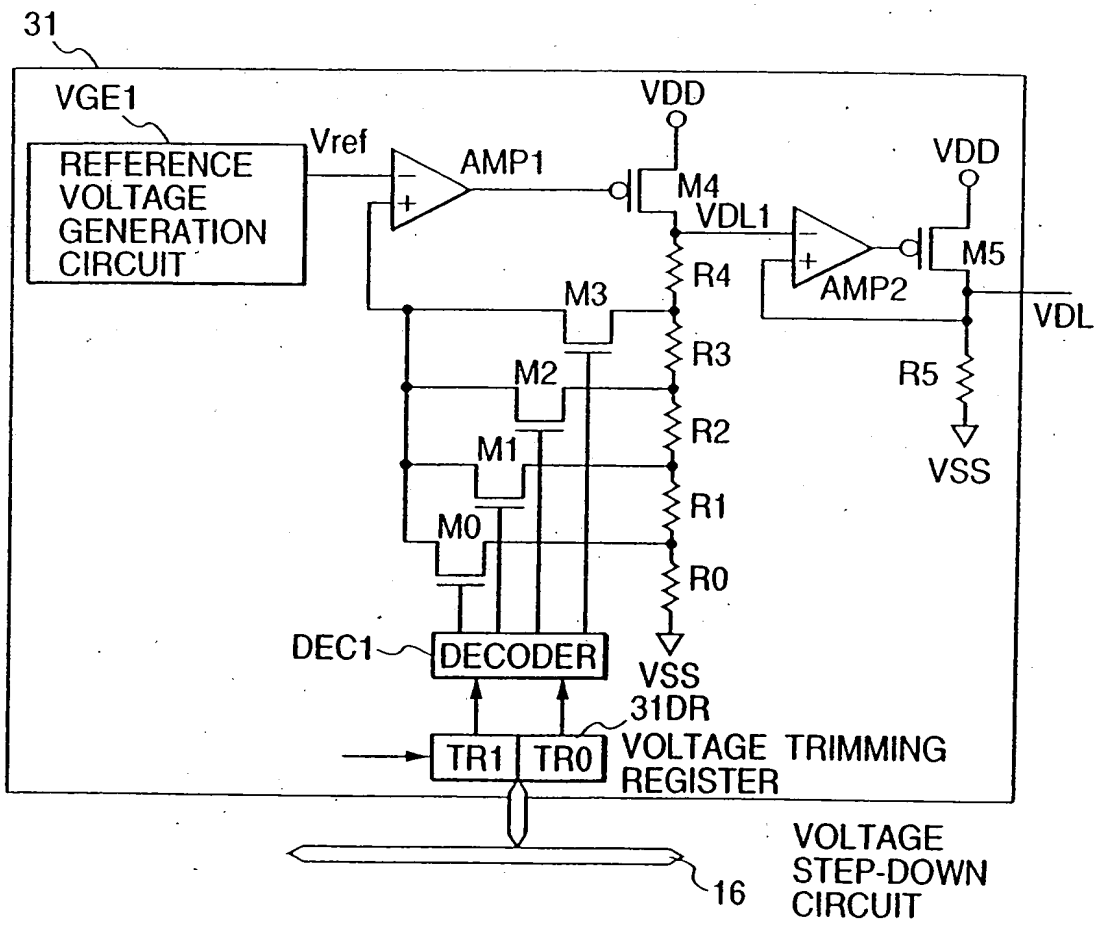

31
VGE1
REFERENCE VOLTAGE GENERATION CIRCUIT
Vref
AMP1
VDD
M4
VDL1
VDD
M5
AMP2
VDL
R4
M3
R3
M2
R2
M1
R1
M0
R0
R5
VSS
DEC1
DECODER
VSS
31DR
TR1
TR0
VOLTAGE TRIMMING REGISTER
VOLTAGE STEP-DOWN CIRCUIT
16

FIG. 22

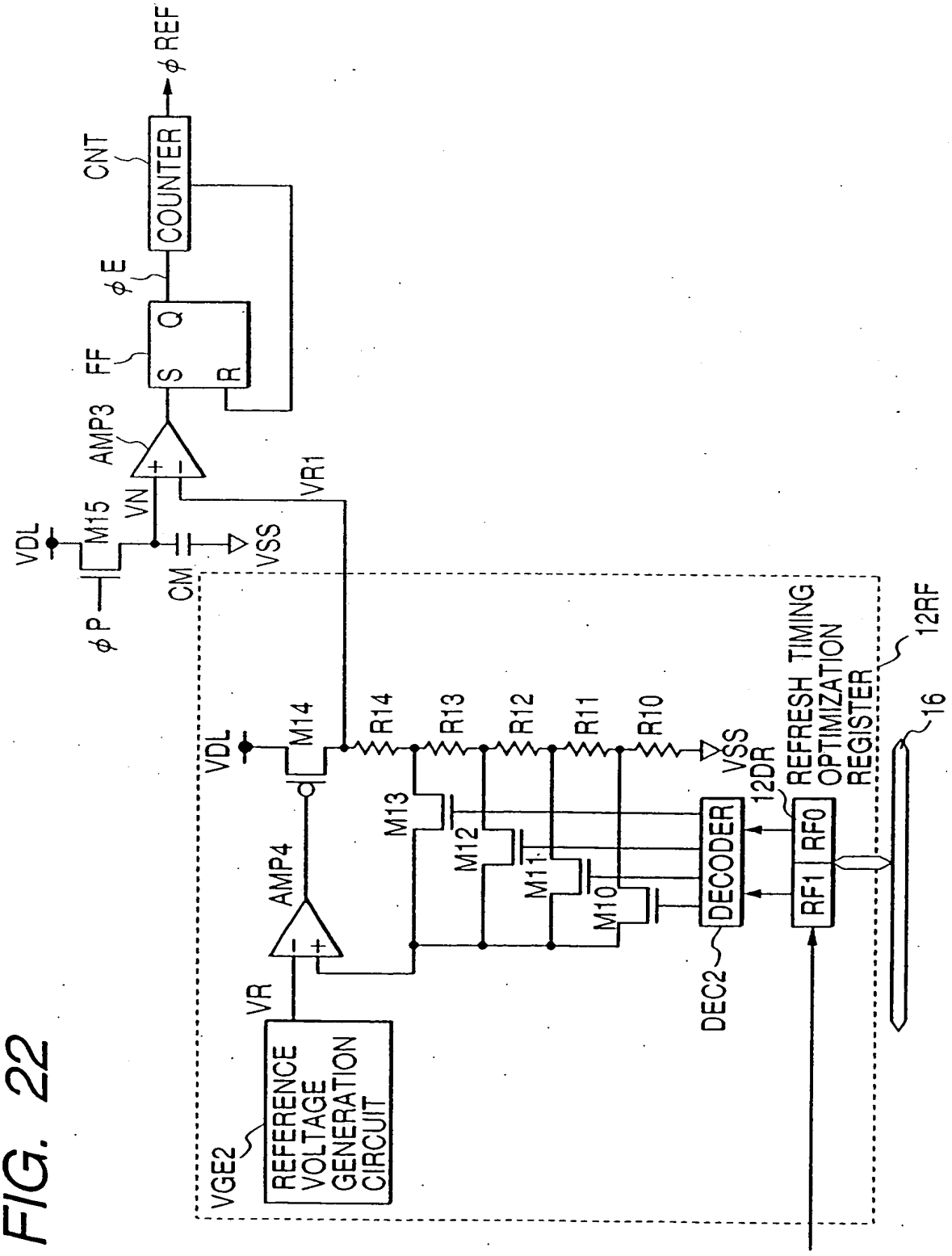

φREF
CNT
COUNTER
φE
FF
Q
S
R
AMP3
VR1
VDL
M15
VN
VSS
CM
φP
M14
R14
R13
R12
R11
R10
VSS
M13
M12
M11
M10
AMP4
VR
DECODER
12DR
REFRESH TIMING OPTIMIZATION REGISTER
RF1
RF0
12RF
16
DEC2
REFERENCE VOLTAGE GENERATION CIRCUIT
VGE2

FIG. 23

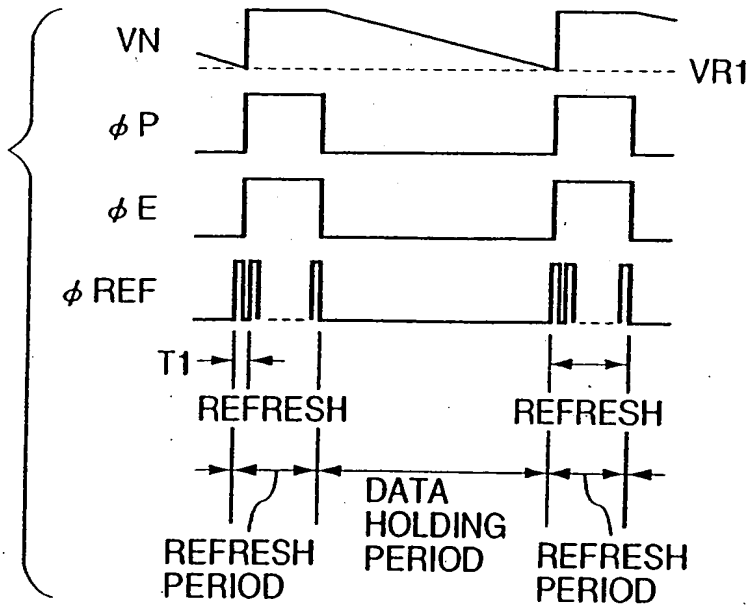

VN
VR1
φP
φE
φREF
T1
REFRESH
REFRESH
DATA
HOLDING
PERIOD
REFRESH
PERIOD
REFRESH
PERIOD

FIG. 24

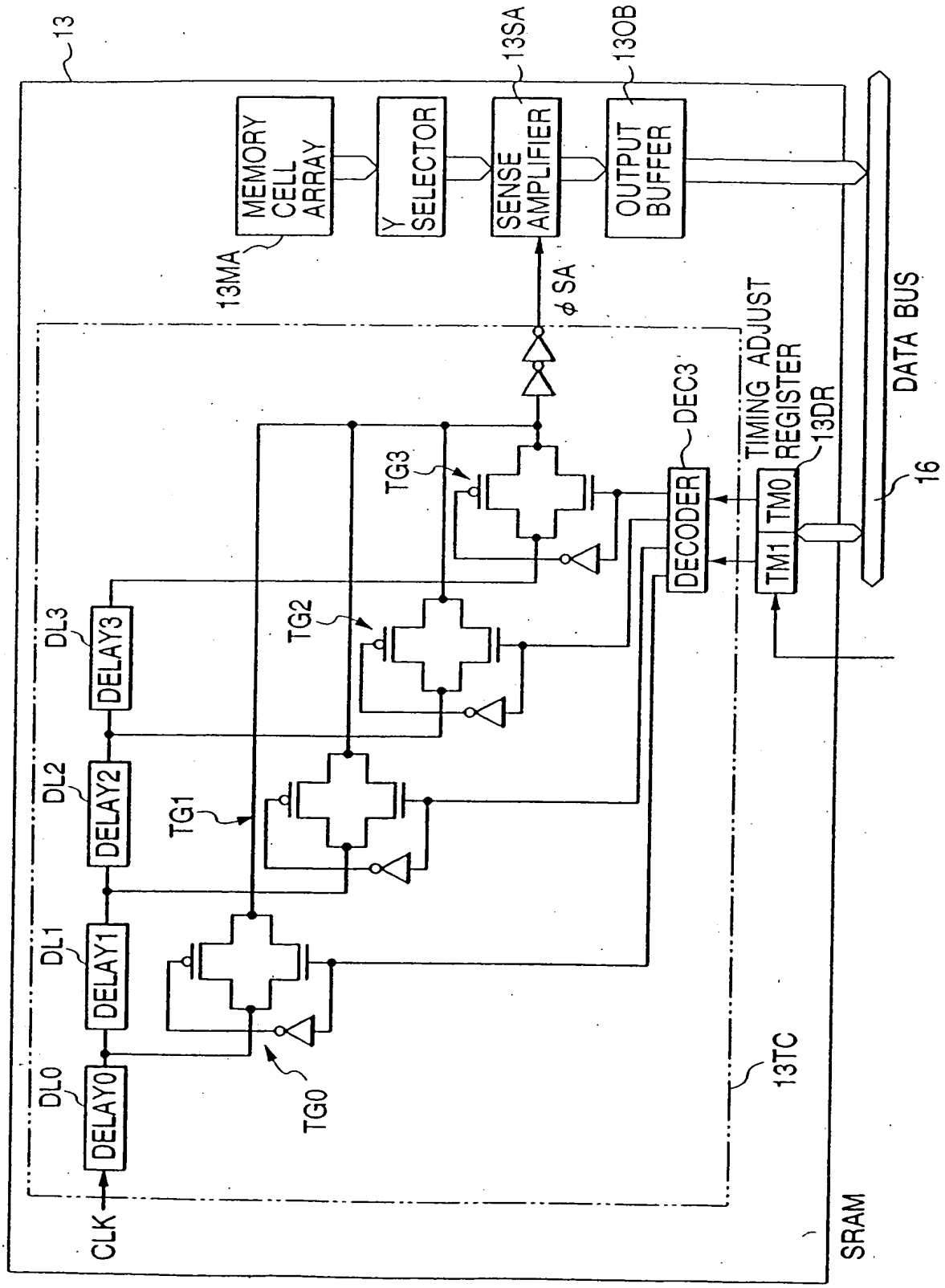
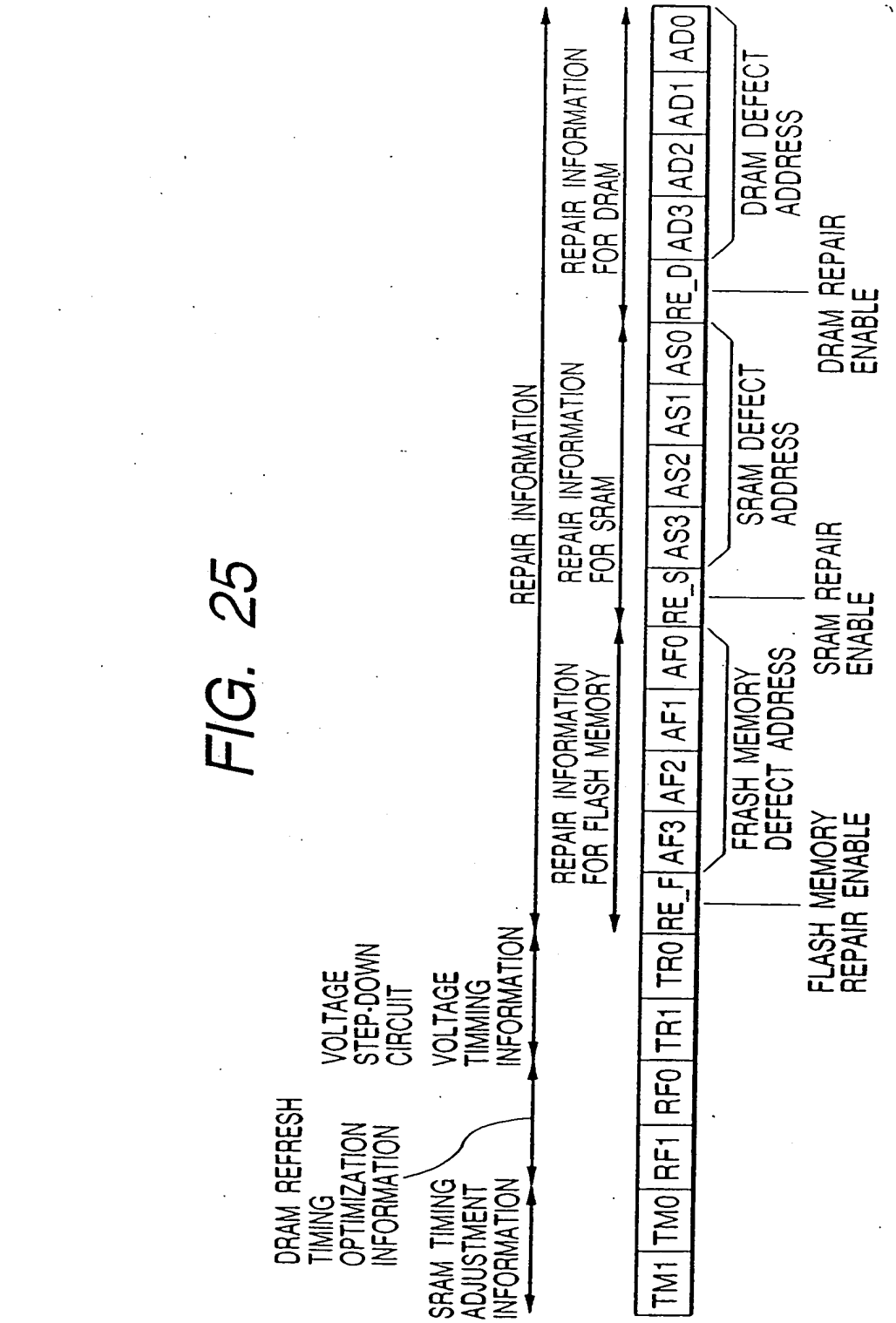

13
MEMORY CELL ARRAY
13MA
Y SELECTOR
SENSE AMPLIFIER
13SA
OUTPUT BUFFER
13OB
DATA BUS
16
φ SA
TIMING ADJUST REGISTER
13DR
TM0
TM1
DEC3
DECODER
TG3
TG2
TG1
TG0
DL3
DELAY3
DL2
DELAY2
DL1
DELAY1
DL0
DELAY0
CLK
13TC
SRAM

FIG. 25


DRAM REFRESH TIMING OPTIMIZATION INFORMATION
VOLTAGE STEP-DOWN CIRCUIT
SRAM TIMING ADJUSTMENT INFORMATION
VOLTAGE TIMMING INFORMATION
REPAIR INFORMATION
REPAIR INFORMATION FOR FLASH MEMORY
REPAIR INFORMATION FOR SRAM
REPAIR INFORMATION FOR DRAM
TM1 TM0 RF1 RF0 TR1 TR0 RE_F AF3 AF2 AF1 AF0 RE_S AS3 AS2 AS1 AS0 RE_D AD3 AD2 AD1 AD0
FRASH MEMORY DEFECT ADDRESS
FLASH MEMORY REPAIR ENABLE
SRAM REPAIR ENABLE
SRAM DEFECT ADDRESS
DRAM REPAIR ENABLE
DRAM DEFECT ADDRESS

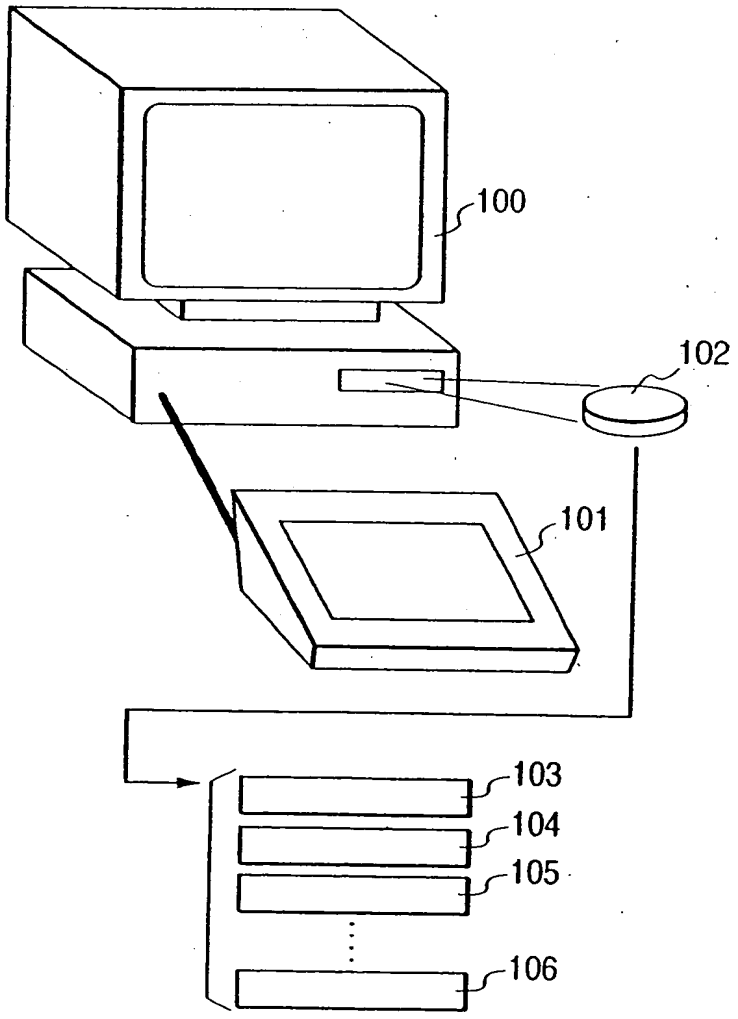



FIG. 26